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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,903	10/28/2003	Koji Muranishi	031948-3	3959

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EXAMINER	
JAGER, RYAN C	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
07/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,903	MURANISHI, KOJI	
	Examiner	Art Unit	
	Ryan C. Jager	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-19* is/are rejected.

7)☒ Claim(s) *2-13,20,21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/27/2007 has been entered.

Claim Objections

2. Claims 2-21 are objected to because of the following informalities:

With respect to claims 13 and 14, it is suggested the recitation "the selected clock" on line 9, be changed to --a selected clock--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Pan (USP 6348823).

With respect to claim 14, figure 7A of Pan discloses a phase adjustment circuit receives a first pair of clock signals (704, 708) and outputs a second pair of clock signals (710,708) with phases satisfying a predetermined condition to a central processing unit, comprising:

a clock proliferator (734) receives a first clock signal (704) and generates a plurality of clock signals therefrom (outputs from 734 to 732);

a clock selector (732) receives said plurality of clock signals from the clock proliferator, selects one of the received plurality of clock signals in accordance with a selection signal (726), and outputs the selected clock signal (710); and

a phase difference detector (612) that receives the selected clock signal (710) and a second clock signal (708) differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal (714) indicating whether the predetermined condition is satisfied;

the first clock signal (704) and the second clock signal (708) constituting the first pair of clock signals;

the second clock signal (708) and the selected clock signal (710) constituting the second pair of clock signals.

wherein the selected clock signal (710) has a higher frequency than the second clock signal (708), and the predetermined condition specifies that rising and falling edges (there are rising and falling edges of the second clock (708) that occur when the selected clock (710) is high) of the second clock signal occur while the selected clock signal is high.

*Note that the limitation of providing the output clocks to a CPU is recited in the preamble and is considered a statement of intended use. The circuit disclosed in figure 7A of Pan is fully capable of providing clocks to a CPU and the limitation is met.

With respect to claim 15, figure 7A of Pan discloses the phase adjustment circuit of claim 14, wherein the clock proliferators generates the plurality of clock signals by delaying the first clock signal by different amounts (shown if fig. 8A element 734).

With respect to claim 16, figure 7A of Pan discloses the phase adjustment circuit of claim 15, wherein the clock proliferators comprises a cascaded plurality of delay elements (see figure 8A element 734).

With respect to claim 17, figure 7A of Pan discloses the phase adjustment circuit of claim 14, further comprising:

an external input terminal for input of the selection signal (726); and

an external output terminal for output of the detection signal (714).

With respect to claim 18, figure 7A of Pan discloses the phase adjustment circuit of claim 14, further comprising:

an externally writable register (728) that stores the selection signal (726) and providing the selection signal to the clock selector; and

an external output terminal for output of the detection signal (726).

With respect to claim 19, figure 7A of Pan discloses the phase adjustment circuit of claim 14, further comprising a selection signal generator (730 and 606) that receives the detection signal (714) and generates the selection signal (SUM).

Allowable Subject Matter

4. Claim 2-13 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

5. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Jager whose telephone number is (571) 272-7016. The examiner can normally be reached on M-F 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bob Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan C. Jager/
7/10/2007

Kenneth B. Wells
Primary Examiner